UG-2864ASYDT01

Evaluation Kit User Guide

Writer:

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Version: Preliminary

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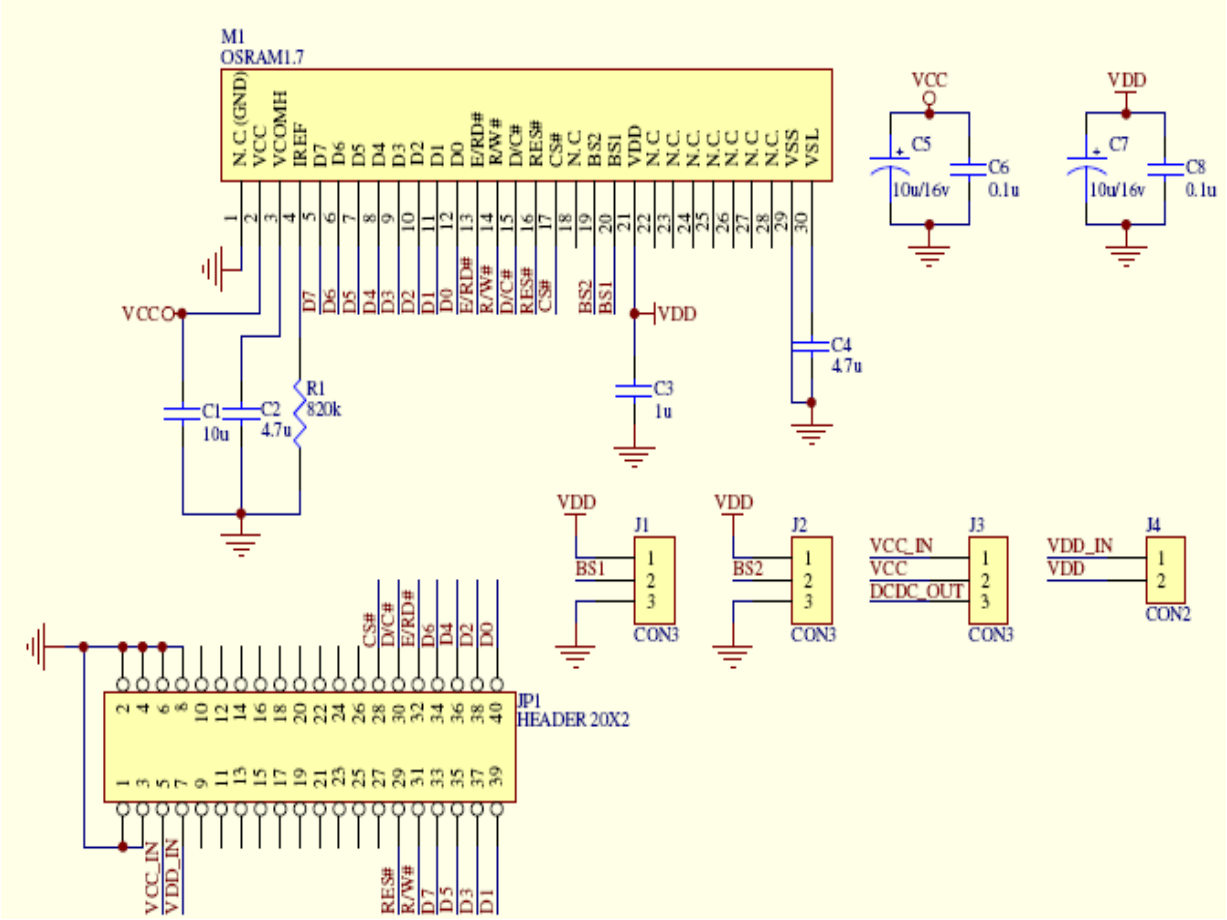
1.REVISION HISTORY

Date	Page	Contents	Version
200X/XX/XX		Preliminary	Preliminary 0.0

2.EVK Schematic



3.Symbol define

D0-D7：These pins are 8-bit bi-directional data bus to be connected to the microprocessor`s data bus. When serial mode is selected,D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.

E/RD#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is will be used as the Enabl(E) signal. Read/write openation is initiated when this pin is pulled high and CS# is pulled low.When connecting to an8080-microprocessor, This pin receives the Read(RD#)signal.Data read operation is initiated when this pin is pulled low and CS# is pulled low.

W/R# : This pin in MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write(R/W#)selection input. Pull this pin to “High”for read mode and pull it to ”LOW” for write mode. When 8080 interface mode is selected, this pin will be the Write(W/R#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.

D/C# : This pin is Data/Command control pin. When the pin is pulled high, the input at D7-D0 is treated as display data. When the pin is pulled low, the input at D7-D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

RES# : This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS# : This pin is the chip select input. The chip is enabled for MCU communication only CS# is pulled low.

BS1,BS2 : These pins are MCU interface selection input. See the following table:

	6800-parallel interface	8080-parallel interface
BS0	0	0
BS1	0	1
BS2	1	1

VCC : This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.

VDD : This is a voltage supply pin. It must be connected to external source.

VSS : This is a ground pin. It also as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

VSL : This pin the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and Vss.

NC : These pins should be left open individually.

4.TIMMING CHARACTERISTICS

4.1 80-Series MPU parallel Interface

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 1 80-Series MPU parallel Interface Timing Characteristics

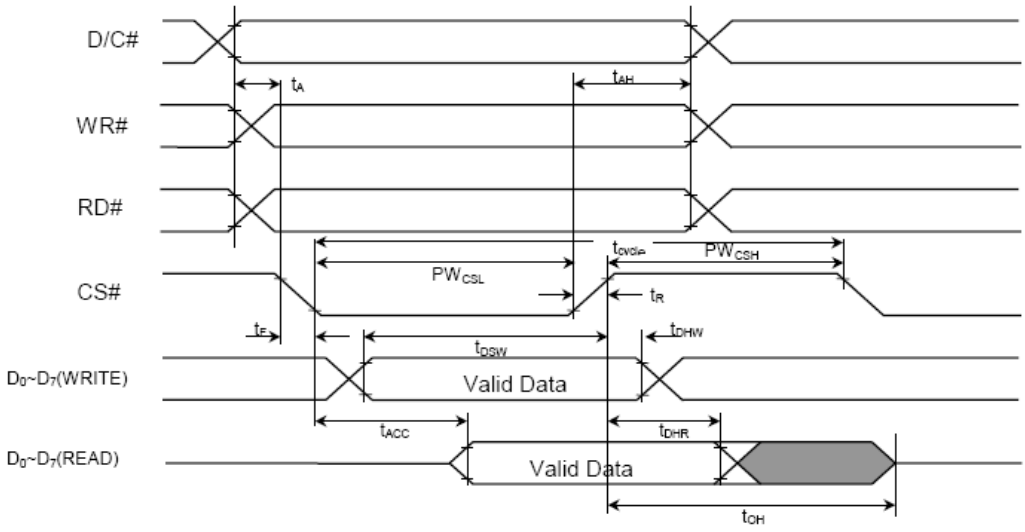


Figure 1 80-Series MPU parallel Interface Timing Diagram

4.2 6800-Series MPU parallel Interface

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 1 80-Series MPU parallel Interface Timing Characteristics

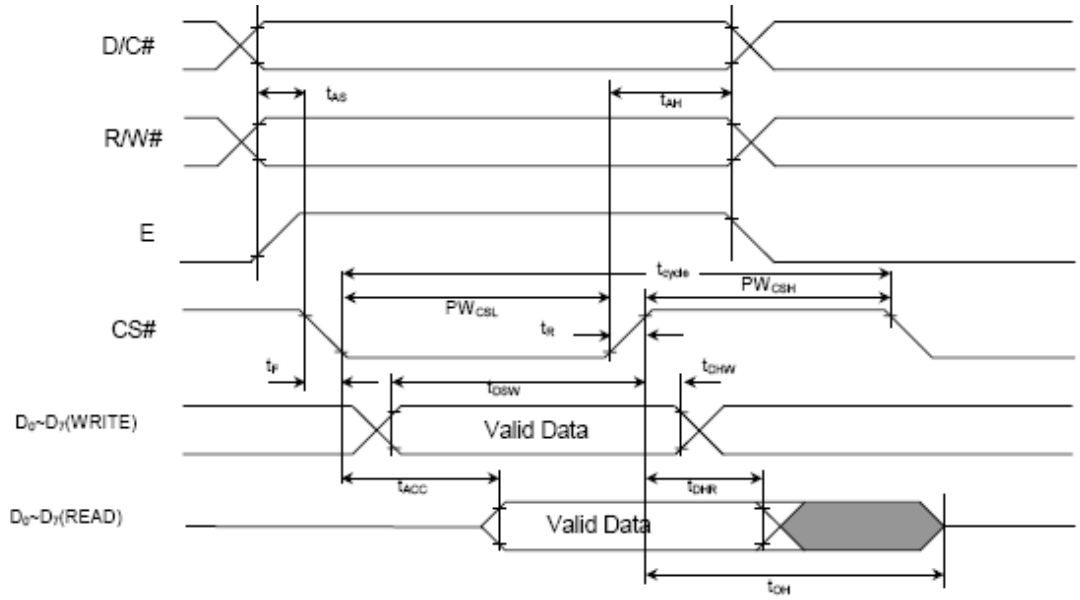


Figure 1 80-Series MPU parallel Interface Timing Diagram

5.EVK use introduction

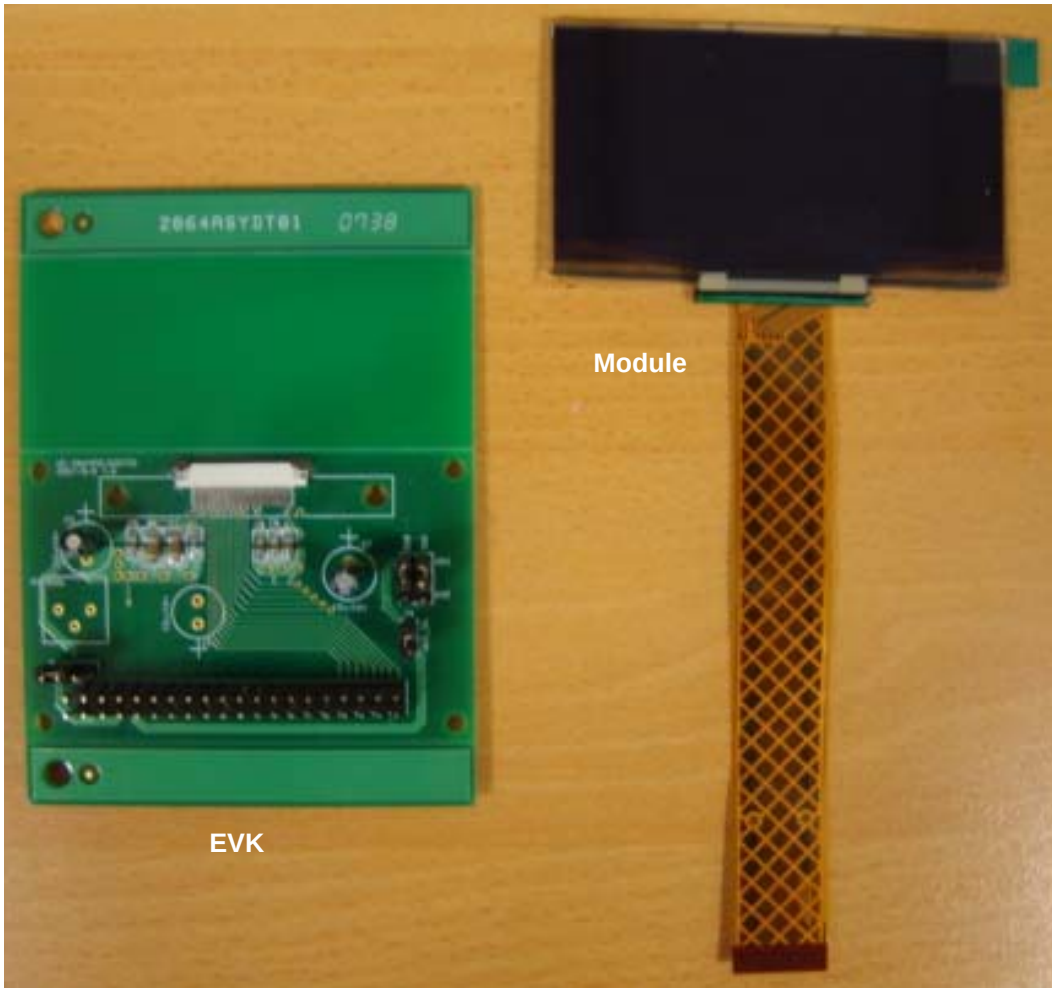


Figure 5 EVK PCB and OLED Module

UG-2864ASYDT01 is (TAB+FPC) type module, please refer to Fig5, Fig6.User can use leading wire to connect EVK with customer's system. The example shows as Fig7.

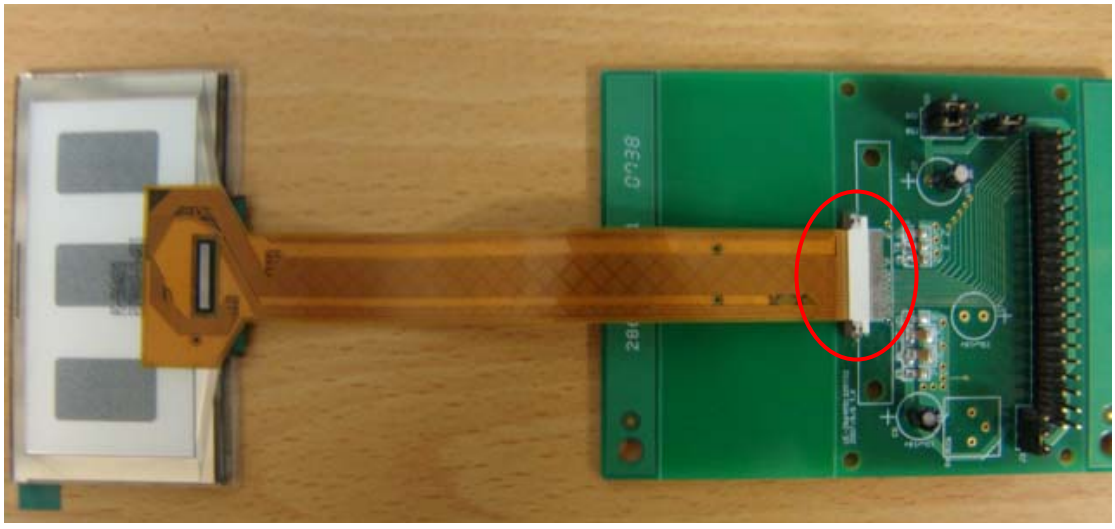


Figure 6 The combination of the module and EVK

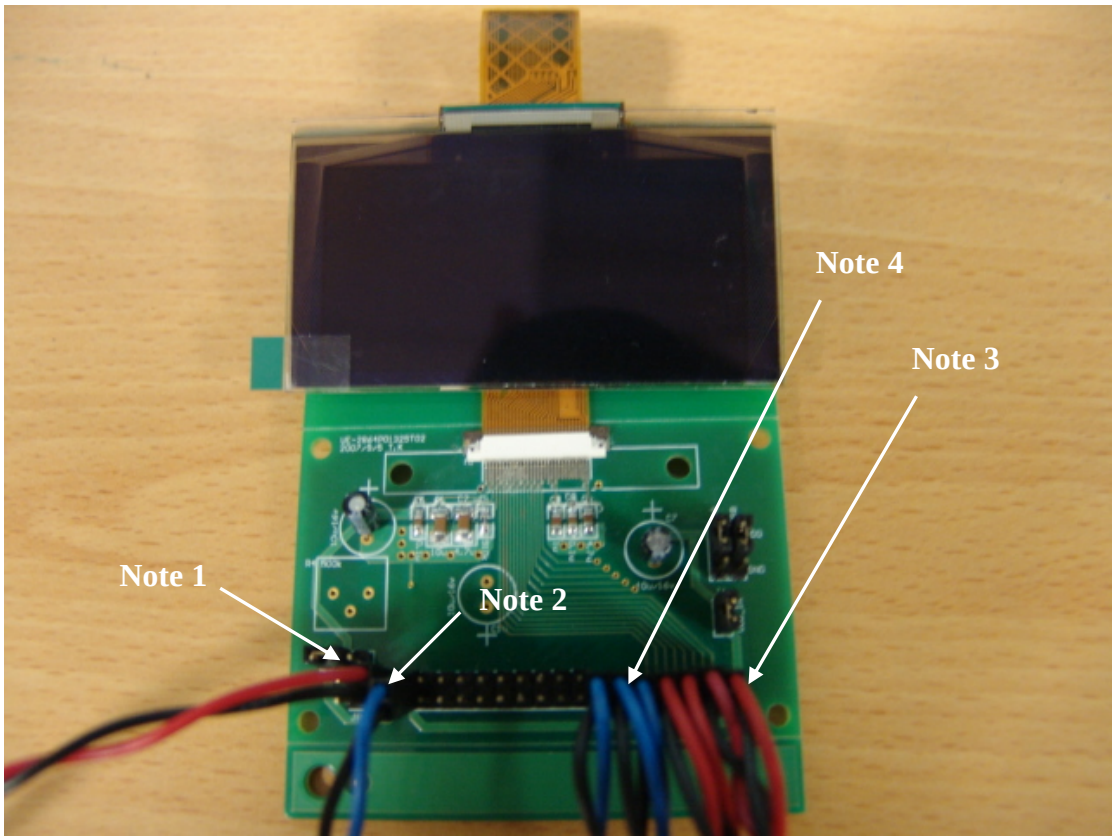


Fig 7 EVK with test platform

Note 1：It is OLED high voltage supply.

Note 2：It is logic voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin.(D0-D7)

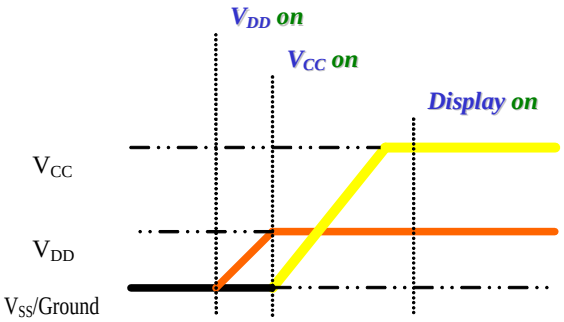
Note 4：Those are leading wire connect to control board. Those are control pin.
(A0,CSB,RDB,WRB,RSTB)

6.Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

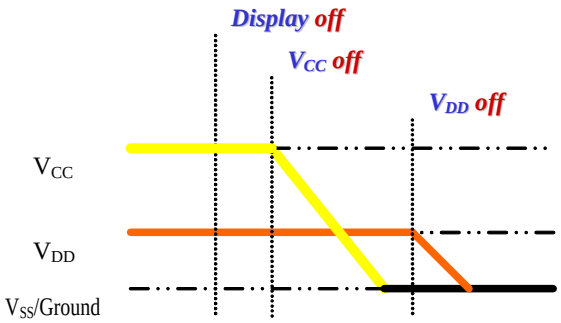
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



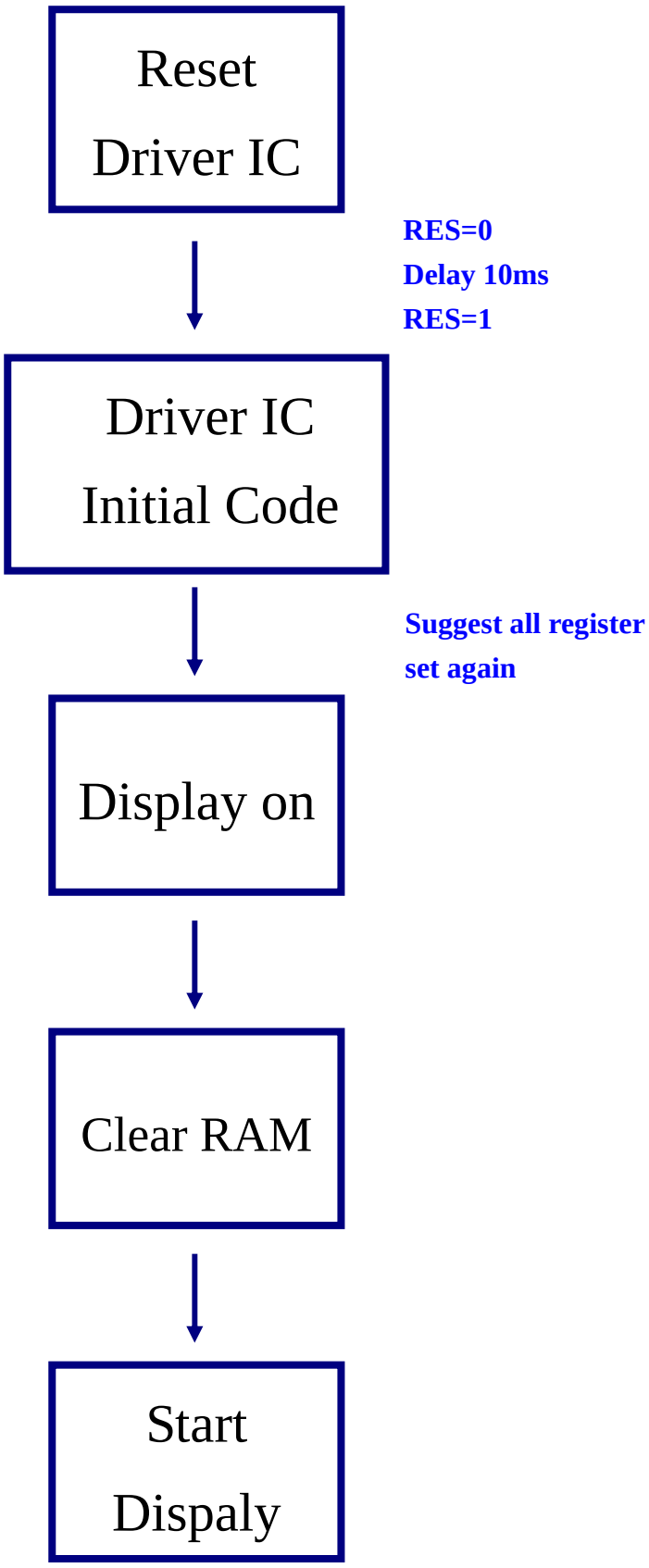
Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



7.How to use SSD1325 module

7.1 Initial Step Flow



7.2 RD recommend Initial Code for 80 Interface: